In re Patent Application of:
RUAT ET AL.
Serial No. **10/824,932**
Confirmation No. **7552**
Filed: **APRIL 15, 2004**

In the Claims:

1. (Currently Amended) An asynchronous frame receiver comprising:

an input to receive ~~for receiving~~ asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

a first state machine configured as a break character detection unit to detect ~~for detecting~~ the break character; ~~and~~

a second state machine configured as a standard character processing unit to detect ~~for detecting~~ the standard characters; and ~~characters, said standard character processing unit being activated by said break character detection unit based upon the break character being detected.~~

said first and second state machines being further configured so that

in a first operating mode only said standard character processing unit is to operate, and

in a second operating mode both said first and second state machines are to operate, with said break character detection unit to activate said standard character processing unit after the character break has been detected.

2. (Original) An asynchronous frame receiver according to Claim 1, further comprising a selection circuit for selecting a first operating mode in which said break character

detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit.

3. (Original) An asynchronous frame receiver according to Claim 1, wherein said break character detection unit detects a break character formed of bits having a same value.

4. (Original) An asynchronous frame receiver according Claim 1, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

5. (Original) An asynchronous frame receiver according to Claim 4, further comprising a self-synchronization circuit for synchronizing a local clock signal of the receiver with a reference clock signal in the synchronization character.

6. (Original) An asynchronous frame receiver according to Claim 5, wherein said self-synchronization circuit is activated by said break character detection unit.

Claim 7 (Cancelled).

8. (Original) An asynchronous frame receiver according to Claim 2, wherein said selection circuit comprises a register for storing a mode bit.

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9. (Original) An asynchronous frame receiver according to Claim 1, further comprising a substrate, and wherein said break character detection unit and said standard character processing unit are on said substrate so that the receiver comprises an integrated circuit.

10. (Currently Amended) A microcontroller comprising:

a universal asynchronous receiver transceiver (UART) comprising

an input to receive ~~for receiving~~ asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters,

a first state machine configured as a break character detection unit to detect ~~for detecting~~ the break character, ~~and~~

a second state machine configured as a standard character processing unit to detect ~~for detecting~~ the standard characters, ~~said standard character processing unit being activated by said break character detection unit based upon the break character being detected,~~ and

said first and second state machines being further configured so that

in a first operating mode only said standard character processing unit is to operate, and

in a second operating mode both said first and second state machines are to operate, with said break character detection unit to activate said standard character processing unit after the character break has been detected; and

a processor connected to said UART.

11. (Original) A microcontroller according to Claim 10, wherein said UART further comprises a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit.

12. (Original) A microcontroller according to Claim 10, wherein said break character detection unit detects a break character formed of bits having a same value.

13. (Original) A microcontroller according Claim 10, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

14. (Original) A microcontroller according to Claim 13, wherein said UART further comprises a self-synchronization circuit for synchronizing a local clock signal of said UART receiver with a reference clock signal in the synchronization character.

15. (Original) A microcontroller according to Claim 14, wherein said self-synchronization circuit is activated by said break character detection unit.

Claim 16 (Cancelled).

17. (Original) A microcontroller according to Claim 11, wherein said selection circuit comprises a register for storing a mode bit.

18. (Currently Amended) A method for processing asynchronous frames in an asynchronous frame receiver, the method comprising:

receiving as input by the asynchronous frame receiver the asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

detecting the break character in the asynchronous frames using a first state machine configured as a break character detection unit; ~~and~~

activating a second state machine configured as a standard character processing unit based upon the break character detection unit detecting the break ~~character.~~ character; and

the first and second state machines being further configured so that

in a first operating mode only the standard character processing unit is to operate, and

in a second operating mode both the first and second state machines are to operate, with the break character detection unit to activate the standard character processing unit after the character break has been detected.

19. (Original) A method according to Claim 18, wherein the asynchronous frame receiver comprises a selection circuit for selecting a first operating mode in which the break character detection unit is deactivated, or a second operating mode in which the break character detection unit is active and controls the standard character processing unit.

20. (Original) A method according to Claim 18, wherein the break character detection unit detects a break character formed of bits having a same value.

21. (Original) A method according Claim 18, wherein the asynchronous frames comprise a synchronization character, and

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wherein the break character detection unit detects the synchronization character.

22. (Original) A method according to Claim 21, wherein the asynchronous frame receiver further comprises a self-synchronization circuit for synchronizing a local clock signal of the asynchronous frame receiver with a reference clock signal in the synchronization character.

23. (Original) A method according to Claim 22, wherein the self-synchronization circuit is activated by the break character detection unit.

Claim 24 (Cancelled).